AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on page 10, line 11, with the following paragraph:

Different circuit implementation is adapted to provide an automatic, on -chip biasing of the peaking amplifier transistors. According to one embodiment of the invention, biasing circuit 120 may include, but is not limited to, a current mirror adapted to bias reference FET 122 to a particular current density, as illustrated in FIG. 1B. The gate voltage of reference FET 122 is used to determine the gate voltage of the peaking amplifier transistor 126. Accordingly, voltage offset circuitry 124 includes two parallel resistors coupled to a buffer to determine a gate voltage for the peaking amplifier transistor 126 using offset voltage 128 and V_g of the reference FET 122. In one embodiment, a voltage divider is used to calculate and determine the gate voltage for the peaking amplifier transistor 126. Additionally, the voltage offset circuitry may include feedback amplifier 130 to select the gate voltage for the peaking amplifier transistor 126. In one embodiment, if the device parameters of the peaking amplifier transistor have changed, the gate voltage needed for the peaking amplifier transistor to operate in an ON mode may need to be changed. Accordingly, amplifier ~~126is~~ 126 is provided with a bias voltage determined from the reference FET 122 and voltage offset circuitry 124. Similarly, if the peaking amplifier transistor 126 is operating in the correct mode, feedback amplifier 130 on die 100 continues to [[be]] provide the same gate voltage to peaking amplifier transistor 126, as illustrated by a feedback loop to the amplifier.